

Gregg Squires
#3

LOW COST COMPUTER
MEETING OUTLINE

- I. OBJECTIVES
- II. MAJOR FEATURES
- III. ACCOMPLISHMENTS
- IV. COST
- V. AVAILABILITY
DETAILED SCHEDULE
- VI. UNRESOLVED ISSUES
- VII. MAJOR SUPPORT
SOFTWARE
MECHANICAL ENGINEERING
LSI
- VIII. DISCUSSION
- IX. ACTION ITEMS

LOW COST COMPUTER

MAJOR OBJECTIVES

- SIGNIFICANTLY ACCELERATE THE PRODUCT DEVELOPMENT SCHEDULE
CURRENT SCHEDULE: BEGIN PRODUCTION MAY 1983*
LOW RISK SCHEDULE: BEGIN PRODUCTION 4/15/84
- PRODUCE AS MANY UNITS IN 1983 AS POSSIBLE
CURRENT PLAN: 400,000**
MONTEREY: 200,000
INITIAL PLAN: 85,000
- AGGRESSIVE COST REDUCTION
CURRENT A400 COST \$127.65 PARTS AND DIRECT LABOR
1983 CRAZY 8 OBJECTIVE: \$ 80.00 OFF-SHORE PARTS AND
DIRECT LABOR
CURRENT CRAZY 8 EST.: \$ 73.46 OFF-SHORE PARTS AND
DIRECT LABOR
1984 COST OBJECTIVE: \$ 65.00

* ORIGINAL LAB COMMITMENT: PROBABLE, 3RD QUARTER, 1983
DEFINITE, 4TH QUARTER, 1983

** BUILT AND IN PIPELINE

MAJOR OBJECTIVES

(CONTINUED)

- OFF-SHORE MANUFACTURE
- SIGNIFICANTLY REDUCE I.C. COUNT
 - A400: 30 I.C.s
 - INITIAL CRAZY 8: 12 I.C.s
 - CRAZY 8: 10 I.C.s
- PUT AS MANY DESIRABLE CONSUMER FEATURES AS POSSIBLE

LOW COST COMPUTER

MAJOR FEATURES

- TYPEWRITER STYLE KEYBOARD 3/4 STROKE
- SMALL SIZE, LIGHTWEIGHT
- SOFTWARE, HARDWARE, AND STYLING COMPATIBLE TO 1200XL
- 16K MINIMUM - 64K MAXIMUM (INTERNAL)
- 24K ROM - INCLUDING ATARI BASIC
- HELP KEY AND SELF TEST
- INTERNATIONAL CHARACTER SET
- 2 JOYSTICK CONNECTORS
- OPTIONAL DUST COVER
- MANUFACTURABILITY
 - HOUSING - 2 PIECE CONSTRUCTION
 - PCB - ONE DOUBLE-SIDED
- EXPANSION BUS
 - DIRECT VIDEO
 - PERITEL POSSIBLE
 - 5200 EXTERNAL ADAPTOR POSSIBLE
 - SPECSMANSHIP

LOW COST COMPUTER

ACCOMPLISHMENTS

1. CRITICAL PATH ITEMS ON SCHEDULE
2. SCHEMATIC COMPLETE
3. 1ST WORKING UNIT DELIVERED
4. I.D. COMPLETE
5. MECHANICAL DESIGN FROZEN
6. PRELIMINARY LIST OF MATERIALS COMPLETE
7. COST ESTIMATE COMPLETE (COST OBJECTIVES ARE HOLDING, OR ARE LESS)
8. FRED CHIP DESIGN SIGNED OFF
FRED MASK MAKING BEGUN
9. FRED DOCUMENTATION COMPLETE AND DISTRIBUTED

ACCOMPLISHMENTS

10. KEYBOARD SPEC FROZEN - VENDORS BEING QUALIFIED
11. ALL MECHANICAL DESIGN FROZEN
12. 1ST PASS AT PORKEY CHIP COMPLETE
13. PROVISIONS FOR PAM COMPATIBILITY WITH EXTERNAL ADAPTOR
14. 2ND PCB IN PROGRESS (64K)
15. HAVE EPROMS IN HAND FOR 8K AND 16K
16. GOOD CONTACT WITH MANUFACTURING AND ATARI TAIWAN
17. INTERNATIONAL - PAL AND PERITEL VERIFIED

CRAZY 8: PARTS COST SUMMARY*

VERSION DATE: JANUARY 7, 1983

<u>ITEM</u>	<u>QUANTITY</u>	<u>COST</u>
RESISTORS	71	.368
CAPACITORS	43	2.829
CONNECTORS	38	4.202
PC BOARD	1	6.6
CUSTOM ICs		
***FRED	1	3.85
***PORKY	1	2.5
***SALLY	1	3.25
***ANTIC	1	3.57
***GTIA	1	2.54
***BASIC ROM	1	2.5
***RUFUS	1	5.8
OTHER ICs	8	12.471
MISC. ELECT.	122	2.8602
KEYBOARD	1	8
OTHER MECH	9	3.576
PWR ADAPTOR	1	3.41
OTHER PKOUT	10	3.63
	<hr/>	<hr/>
TOTALS (16K)	311	71.9562

PLUS: DUTIES, SHIPPING, OVERHEAD, AND LABOR (.55 HOURS FINAL
ASSEMBLY AND TEST)

* REVISED VERSION ON 1/14/83

LOW COST COMPUTER

KEY MILESTONES

JANUARY 15	RELEASE OF PRELIMINARY DOCUMENTATION
JANUARY 24	2ND PASS OF PORKEY IC
FEBRUARY 1	MATERIAL ACQUISITION COMPLETELY REVIEWED LONG LEAD TIME ITEMS ORDERED
FEBRUARY 7	SAN JOSE SOFT TOOL COMPLETE
FEBRUARY 8	1ST FRED SILICON
FEBRUARY 14	WORKING UNIT WITH PCB, CUSTOM ICs (I.E., FRED PORKEY) AND OPERATING SYSTEM
FEBRUARY 14	START TOOLING EFFORT IN FAR EAST
FEBRUARY 28	SUBMIT TO LAB FCC CERTIFICATION
MARCH 14	ENGINEERING RELEASE
MARCH 28	2ND FRED SILICON (IF REQUIRED)
APRIL 18	SAN JOSE TEXTURED HARD TOOLS COMPLETE 1ST FAR EAST TOOLS COMPLETE AND SHAKEN DOWN

KEY MILESTONES

(CONTINUED)

MAY 2	BEGIN PRODUCTION
JULY 15	2ND FAR EAST TOOL SET ON LINE
AUGUST 15	3RD FAR EAST TOOL SET ON LINE
SEPTEMBER 15	4TH FAR EAST TOOL SET ON LINE

LOW COST COMPUTER

UNRESOLVED ISSUES

1. COMMUNICATIONS
2. SOFTWARE SCHEDULE
3. SOFTWARE COMPATIBILITY
4. EXPANSION CONNECTOR
5. ON-BOARD BASIC
6. THERMAL
7. FRED, RAM, & PORKEY
8. BATTERY ELIMINATOR
9. SCREEN DUMP
10. CONDENSED CHARACTER SET
11. PACKAGING AND MANUAL SCHEDULE AND RELATED PRICE OBJECTIVES

UNRESOLVED ISSUES

(CONTINUED)

12. MANUFACTURING ISSUES:

STAGING: WHERE IS IT GOING TO BE BUILT?

HOW MANY DIFFERENT PLACES?

RELEASE QUANTITIES

16K

32K

48K

64K

13. MATERIAL ACQUISITION ISSUES:

STAGING

CONTRACTURAL GUARANTEES

GUARANTEES FOR RELEASE

14. INTERNATIONAL - SECAM

15. ENTIRE SCHEDULE COULD SLIP 6 WEEKS IF 1ST PASS FRED DOES NOT WORK

16. MAY NEED QUICK TURN ROMs FOR O.S.

17. TOOLING

BURN-IN OVENS

18. NAME OF PRODUCT

* ATARI CONFIDENTIAL *

PRELIMINARY

Atari 600 Home Computer

Liz: Low Cost Computer Specification

Revision One: 9/17/82

Revision Two: 1/07/83

*How to ASIC
activate key
hold key
fill screen.*

This specification will identify design goals and limitations. The emphasis will be on engineering details and marketing.

-Price Goals

The price goal for Liz is \$200. The cost of manufacture will be less than \$75. For its price point, Liz has features and capabilities exceeding competitors products.

Design Goals:

Liz has a full size keyboard, with full stroke feel. Other features will be the Atari Serial Bus, Atari Custom Video Chips, either a new 16K or the Atari 800 10K ROM Operating System Rev. B, 16K RAM, and the possibility of expansion via card edge fingers accessible at the rear of the unit. The Fred custom chip will make possible a low-cost PAM adaptor, which would include, in an external unit, PAM controller interface, and PAM O/S ROMS.

Major cost reductions will be due to:

- (a) Single P.C. Board construction.
- (b) Greater circuit integration, reducing the total chip count to 9 LSI.
- (c) Less memory space decoding while allowing unlimited memory expansion by external circuitry.
- (d) Simple packaging, fewer connectors, fewer parts.
- (e) Low-Cost keyboard.

Introduction and Scope

The purpose of this document is to detail the engineering design specifications and the engineering performance specifications for the Atari 600 Home Computer. The Atari 600 is a low cost personal computer intended for use in a domestic environment. The Atari 600 is an enhanced version of the Atari 800 computer system. It is reduced in size, lower in price and upward compatible with the Atari 800.

The Atari 600 has been referred to as the Liz, Crazy 8, and S-8 in other documents.

Relevant Documents

Marketing Requirements Statement: Low Cost CPU
#A-SE-05-82-5-0

Atari 800 Hardware Manual (C016555)

Serial Input/Output Interface Ace Under's Handbook Part 1 & 2

De Re Atari

Electrical Requirements for the Liz Keyboard

Liz Schematics

The 6502 Microprocessor Manual

MC68B21 (PIA) Data Sheets

Preliminary Atari 600 Keyboard Specification.

6502 Software Design Manual

6502 Modified Electrical Specifications (C014806)

MTBF Calculations for Atari 800/400 by Steve Zyski (HCD QA Document)

Electrical Details of Atari Custom Chips (uncontrolled documents)

Product Overview

Liz is an 8 bit CPU with the design emphasis on cost reduction. Its design is to extend the Atari home computer product line offering a low-cost, entry level CPU. It will

offer Atari's high quality graphics and sound and will take advantage of Atari's growing software base.

The Atari 600 in comparison with the Atari 1200

The Atari 600 external features differ from those of the Atari 800 in the following areas:

1. Lower profile than the Atari 1200.
2. Much smaller package.
3. Function keys and status LEDs deleted.
4. An interface to the CPU bus (called the Parallel Bus Interface, FBI) has been added. In addition to the standard serial bus interface.
5. The external power supply.
6. The single cartridge slot is on the top (behind the keyboard) instead of the side.
7. The 5 pin DIN connector for the monitor interface has been deleted.
8. Use of Custom LSI to reduce parts count.

Internally the Atari 600 further integrates a single logic board. A custom LSI integrated circuit (Fred) replaces most of the discreet semiconductors required by the 1200 to achieve cost reduction goals and improve manufacturability, reliability and performance.

Externally, the package is two piece, top and bottom housing, for simple assembly and low cost.

The architecture of LIZ is similar to that of the A800 and A1200, with a few significant differences.

The heart of the unit is still the modified 6502 microprocessor Sally.

Later versions of the LIZ unit will have the Antic and GTIA chips integrated into one LSI chip. Until this integration is performed, the display circuits will utilize the standard Antic and GTIA chips.

I/O processing is handled similarly to the A800 and A1200. Forky and a 6520 are used for serial bus and controller interfacing. Keyboard scanning is also performed by the Forky chip, while some FBI handshaking is handled by the PIA(6520).

Memory Configurations

The Atari 600 will be available in two configurations:

1. A 16K Atari 600 (a 600 with 16K of system RAM).
2. A 64K Atari 600 (a 600 with 64K of system RAM).

Upgrade of the 16K to a 64K unit is possible by adding memory chips and an address decoder chip.

Other than memory size, the two versions of the Atari 600 will be identical. The 64K RAM version can use 64K X 1 DRAMs for further cost reduction.

Architecture Overview

The architecture of the Liz Computer is similar to that of the Atari 800. Figure XX shows the basic functional blocks.

The 6502 microprocessor (Atari part #CD14806) is used as the central processing unit (CPU).

The memory, the I/O processing circuitry, the display circuitry, the FBI and the cartridge lie within the memory map of the CPU.

The CPU can address these functional blocks and exchange control/status information and/or data with them.

The operating system of the Liz computer (described in Chapter 6)

controls information exchange between all entities on the CPU bus.

The video display generation circuitry consists of ANTIC, the GTIA, and associated circuitry.

ANTIC is a custom microprocessor with an instruction set geared towards display processing

(alphanumeric and graphic). This is the only device in the 600 that can halt the CPU and become a master on the CPU bus.

ANTIC does this to retrieve display commands from a shared

data base in the
CPU memory.

ANTIC translates the high level CPU commands to a simple
bit stream for the GTIA.

The GTIA adds color and "player missile" graphics to the
input bit stream and provides outputs suitable for display.
The ANTIC and GTIA interfaces directly to the processor bus
in addition to interfacing with each other.

The I/O circuitry consists of the Porkey I/O chip, the 6502
Peripheral Interface Adapter (PIA) and miscellaneous
circuitry.

The Porky and PIA together control the SIO interface and
the controller
interfaces.

The Porky also performs keyboard scanning while the PIA
generates control signals for the PBI.
Certain parts of the GTIA are also used for I/O control.

The Operating System ROM houses the Atari 600 operating
system.

One 16K XO ROM is used for this purpose.

These ROMs can be disabled via the Fred chip, under program
control, and a different O.S. can be loaded from
peripherals (e.g. disks).

The System Memory consists of up to 64K bytes of Dynamic
Random Access Memories (DRAMs).

The Cartridge Interface accepts standard Atari cartridges,
which can occupy XXXX-XXXX

The Controller Interface hosts user input devices such as
joysticks and paddles.

The SIO Interface provides an interface for intelligent
serial peripherals like disks, cassettes and printers.
Several peripherals can be daisy chained on this interface.

The Parallel Bus interface (PBI) provides an interface for
additional memory and memory mapped.

The Keyboard is XX key full stroke QWERTY typewriter style
keyboard with 66 keys with 10 function keys (including a
HELP key) and a RESET key.

The Liz computer Power Supply is an external "battery
eliminator" type power supply.
It takes 115 Vac as nominal input voltage and produces
supply current for the Atari 600 electronics.
(disks).

PBC Specifications

The specification for the Parallel Bus Connector (PBC) are defined in a separate document.
A preliminary pinout for the connector is attached.

Keyboard Interface

The same as the A1200, A800, etc.-
with Fewer keys than the A1200.
The switch matrix for the keyboard must be different to accomodate the further integration of Pokey in the Porky chip.

Controller Interface

Same as the A1200.

Cartridge Interface

Same as the left cartridge on the A800, with passive chip selects disable of RAMS.

T.V. Interface

Same as the A1200, with RF modulated output as well as composite output for a video monitor.

Digital Logic

6502 CPU - will be the same as SALLY, the custom 6502.

Memory Map - Liz will initially use the 10K ROMS (operating system) of the A800. This means that no software is required, and the unit will run 800/800 software. A major design goal is to have software compatibility with existing Atari products.

RAM - 000 to 3FFFFH (16K)

ROM - D800 to FFFF

I/O - D000-D7FF

Cartridge - A000-BFFF

SPARE - 4000-9FFF, C000-CFFF

There is no self test mode for the LIZ, as in the A1200, but the ROM can be disabled by the FEC. There is also no cartridge control, only 4 parts of the I/O space are decoded.

Antic chip - this chip is explained in the other literature available (A1200 and A800 specs.).

GTIA chip - same as Antic.

PIA chip - Controller inputs are the same as for the A1200 and the A800.

Part D pins are as yet undefined

The rest of the pins are as defined as in the A1200 specs.

Porky chip - functionally the same as Pokey, with CMOS multiplexers integrated on-chip. See Porky specification.

Memory - 16K X 4 DRAMS and 64K X 1 DRAMS may be used (different PCBs are required to accomodate the two types). All multiplexing, timing and control signals are generated by the Fred chip. RAS and CAS are generated as in the 800.

AC Line Interface

The AC line input to the power supply should have the following characteristics:

V=100 Vac (min) 130 Vac (Max)
F=60 Hz \pm 10 cycles

R.F. Modulator

The R.F. Modulator inputs the composite video and the monosural audio signals from the video summation circuitry and produces a modulated signal suitable for the television. A channel selection switch is provided to allow the user to use either TV channel 2 or channel 3 with the S-16.

The modulated signal will have the following characteristics with a 75ohm termination:

Maximum Voltage: 2mV
Minimum Voltage: 1mV

The Atari 600 Memory

O.S. ROMs

The 600 O.S. is resident in one 16K X 8 ROM that is located in address space C000H to FFFFH in the CPU Memory Map.

The ROMs input CPU address lines A0 thru A12 and the chip selects from the Fred Chip and generates data on CPU Data Lines.
(D0 thru D7).

The ROMs require a power input of 5v ($\pm 5\%$).

Dynamic RAMs

The Atari 600 Random Access Memories can be either 8-64K X 1 DRAMs or 2 to 8 16K X 4 DRAMs.

The DRAMs in a 16K S-16 reside in addressed 0000H thru 3FFFFH.

The DRAMs in the 64K S-16 can physically occupy the entire address space of the CPU.

Generation of ROW and COLUMN addresses and other control signals are provided by the Fred Chip.

The TV Interface

The 600 provides an RF Modulated output for direct connection to a TV set.

The RF output is available through a phono plug located on the back of the S-16.

A channel selection is provided on the left side of the S-16. The user may use TC channels 2 or 3 with the S-16.

Direct connection to Audio and Video inputs and outputs are available at the PBC connector.

External Video and Audio inputs may thus be applied and will appear on the television screen (or at the speaker). External Video Monitors and Audio Amplifiers may be interfaced via the PBC.

Mechanical Details

To be specified.

Controller Interfaces

The S-16 provides two controller jack interfaces. Both are functionally and electrically identical. The controller jacks are 9 pin D type male connectors with the following signals:

(see figure XX)

PIN 1 thru PIN 4 are general purpose I/O lines. Each of these lines' direction is individually programmable by writing into the PIA internal registers. When a joystick is connected to the controller jacks, these lines are the FWD (forward), BACK, LEFT and RIGHT inputs respectively providing direction control inputs to the S-16. See (1) and (7) for a discussion on the direction control mechanism for these lines. (1) also describes the configuration of these lines when other input devices such as paddles are connected to these lines.

PIN 5 and 9 are BPOT input and APOT input respectively. These inputs accept the outputs from the potentiometers in the two paddles that can be connected to the controller interfaces.

PIN 6 is the "active low" TRIGGER input from the controllers (eg. joysticks, paddles). These inputs are also designed to accept the light pen signal.

When this line goes low the GTIA LP (Light Pen) Input is pulled low.

See section 5.2.1.3.3 and (1) for details.

PIN 7 is the Vcc output to the controllers. This power output has nominal value of 5 Vdc.

PIN 8 is the GROUND reference for the controllers.

Electrical Levels

PINS 1 through PIN 4 are buffered inputs in parallel with reticod outputs (with static protection circuitry) and have the following electrical characteristics:

Input 0 level ---> -0.5Vdc (min) :::: 0.8Vdc (max)

Input 1 level ---> 2.0Vdc (min) :::: (max)

Output 0 level at 1.6mA ---> VSS (min) :::: 0.4Vdc (max)

Output 1 level at -100microamp ---> 2.4 Vdc (min) :::: Vcc (max)

Capacitance ---> 15pF

Load Current at 2.4Vdc ---> 100 microamps

PINS 5 and 9 are schmitt Trigger inputs with a low threshold of 1 Vdc (max) and a high threshold of 1.7 Vdc (min) and a hysteresis of 0.3 Vdc (min).

The input capacitance is 15 pF.

PIN 6 has the following electrical characteristics:

Logic 0 input Level ---> 0.8 Vdc (max)

Logic 1 Input Level ---> 2.0 Vdc (min)

Input capacitance ---> 15 Pf

The Cartridge Interface

The cartridge interface is a 30 pin 15/30 Dual Readout connector (figure 5.2.11) with the following pin-out:

PIN 1 is the S4 Select output to the cartridge. This line goes low if the RD4 input (PIN A) and RDS (PIN 14) are active and an address between A000H and BFFFH is invoked on the CPU bus.

PIN 12 is the S5 Select output to the cartridge. This line goes low if the RD5 input (PIN 14) is active and an address between 8000H and 9FFFH is invoked on the CPU bus.

PIN A is the RD4 input from the cartridge. If a cartridge uses addresses between A000H and BFFFH it should pull this line high internally. When this line is pulled high the S-16 maps the addresses A000H thru BFFFH to the cartridge.

PIN 14 is RDS input from the cartridge.
If a cartridge uses addressed A000H to BFFFH it should pull this line high internally.
The S-16 O.S. polls this line to sense a cartridge.
If this line is sensed high the S-16 maps the addresses between 8000H and 9FFFH to the cartridge.

PIN 15 is the Cartridge CoNTroL (CCNTL) output to the cartridge.
This output is pulled low if the RD5 is high and an address of the form D5XXXH is invoked on the CPU bus.

PIN S is the Buffered Phase 2 (B02) output to the cartridge. The cartridge may use this clock for its internal timing.

PIN R is the CPU Read/Write output to the cartridge from the CPU.

PINs 5,4,3,2,C,D,E,F,H,J,P,N,K, are CPU Address Outputs A0 thru A12 respectively to the cartridge.
The CPU can address an 8K byte segment of memory resident in the cartridge using these lines.

PINs 10, 9, 8, L, 6, 7, 11, M are the CPU data lines D0 thru D7 respectively.

PIN 13 is the Vcc pin with a nominal voltage of 5Vdc.

PIN B is the GROUND reference to the cartridge.

Electrical Levels

The address Outputs (A0 thru A12), the Data Lines (D0 thru D7) during a CPU write cycle, the R/W output and the B02 Output have the following drive capability:

HIGH STATE: $V=2.7$ Vdc (min); $I=20$ microamps (min source current).

LOW STATE: $V=0.5$ Vdc (max); $I=0.36$ mA (max sink current).

The CCNTL Output, and the Select Lines S4 and S5 have the following drive capability:

HIGH STATE: $V=2.7$ Vdc (min); $I=400$ microamps (min source current)

LOW STATE: $V=0.5$ Vdc (max); $I=8$ mA (max sink current).

The RD4 and RD5 inputs and the data lines (D0 thru D7) during a CPU read cycle should have the drive capability of at least one LSTTL gate.

Package and Appearance

Dimension and Weight

Height - 2.7 inches; Width - 15 inches; Dept - 12.5 inches;
Weight - to be specified.

Package Description

Position of Connectors

Keyboard Description

The Atari S-16 Home Computer has a full stroke QWERTY typewriter style keyboard similar in layout to the Atari 800 Home Computer keyboard. The board has 54 alphanumeric keys (including special characters and controls), a space bar, and 11 function keys.

In addition to the alphanumeric keys, the board as a

CONTROL key, for Control functions, input of Graphics characters and Cursor Control. The board also has a CAPS lock key. A SHIFT key is located on each side of the board near the SPACE bar.

Above the typewriter pad is a series of 11 function keys. The tops of these keys are level with the bezel, but depress below bezel to provide the same tactile feel as the alphanumeric keys. Included in the function keys are START, SELECT, OPTION, the ATARI Logo Key and the BREAK key. At the far left of this strip of keys is the RESET key.

The four remaining Function Keys, F1 thru are user programmable.

There is a label panel directly above the Function Keys. This panel contains one LED (in the case of the 16K version) or three LEDs (in the case of the 64K version). It also contains the key labels for the Function Keys.

On the 16K version of the Atari S-16 Home Computer, the strip is a continuation of the keyboard bezel and is made of the same material as the housing. There is one LED which is used as a POWER ON indicator.

The 64K version of the Atari S-16 Home Computer has a label strip made of plexiglas. There are three LEDs, one of which is the POWER ON indicator; the other two LEDs are activated as specified in Chapter 6. The key labels are not stamped on the bezel underneath the strip.

The keyboard is connected to the mother board by a 15-conductor ribbon cable terminating in a Molex 22-01-2156 connector.

This connector is polarized so that it can be connected in only one way. See "S-16 Keyboard

Electrical Requirements" (Atari P/N C060087) and Keyboard Assembly Drawing (C040046) for complete details of electrical parameters.

Package Colors

The keyboard and bezel is dark brown (Borg Warner Cycloac #T84816).

The plexiglas strip above the function keys on the 64K version is translucent brown. The strip above the function keys on the 16K version is the same color as the housing.

Environmental Requirements

Temperature range: 0 to 40 degrees Centegrade.

The housing is white (Borg Warner Cycloac #KJW86006).

Package Materials

The keyboard and housing is made of ABS plastic.

The keytops of the Function Keys are brushed and formed aluminum nameplate material.

SIO Performance

MAX BAUD RATE 19.2K BAUD

Motor Start line with 180 ohm should pull up to (Vcc-0.2) Volts when "ON".

R.F. Modulator Performance

The R.F. Modulator will have the following characteristics with the 75 Ohm termination:

Maximum Voltage: 2mV
Minimum Voltage: 1mV

The Modulator output is selectable via a switch (on the left side of the S-16) to Channel 2 or Channel 3.

Monitor Jack Performance

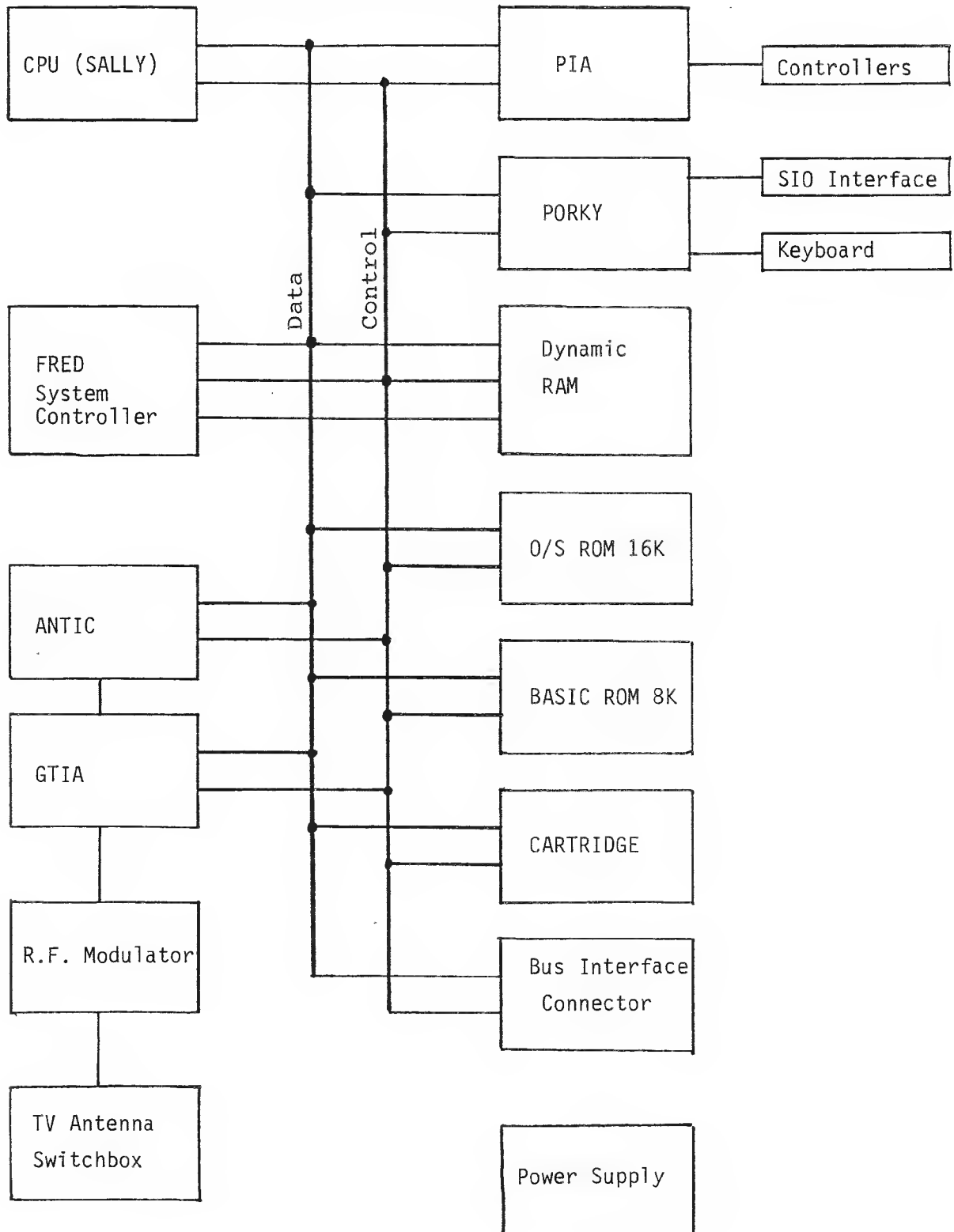
Composite video and composite liminance outputs will have the following characteristics with a 75 ohm termination:

SYNC TIP (MAX) 0.08 V
BLACK LEVEL 0.35 V \pm 10%
WHITE LEVEL 0.7V \pm 15%

Audio Outputs will have the following characteristics:

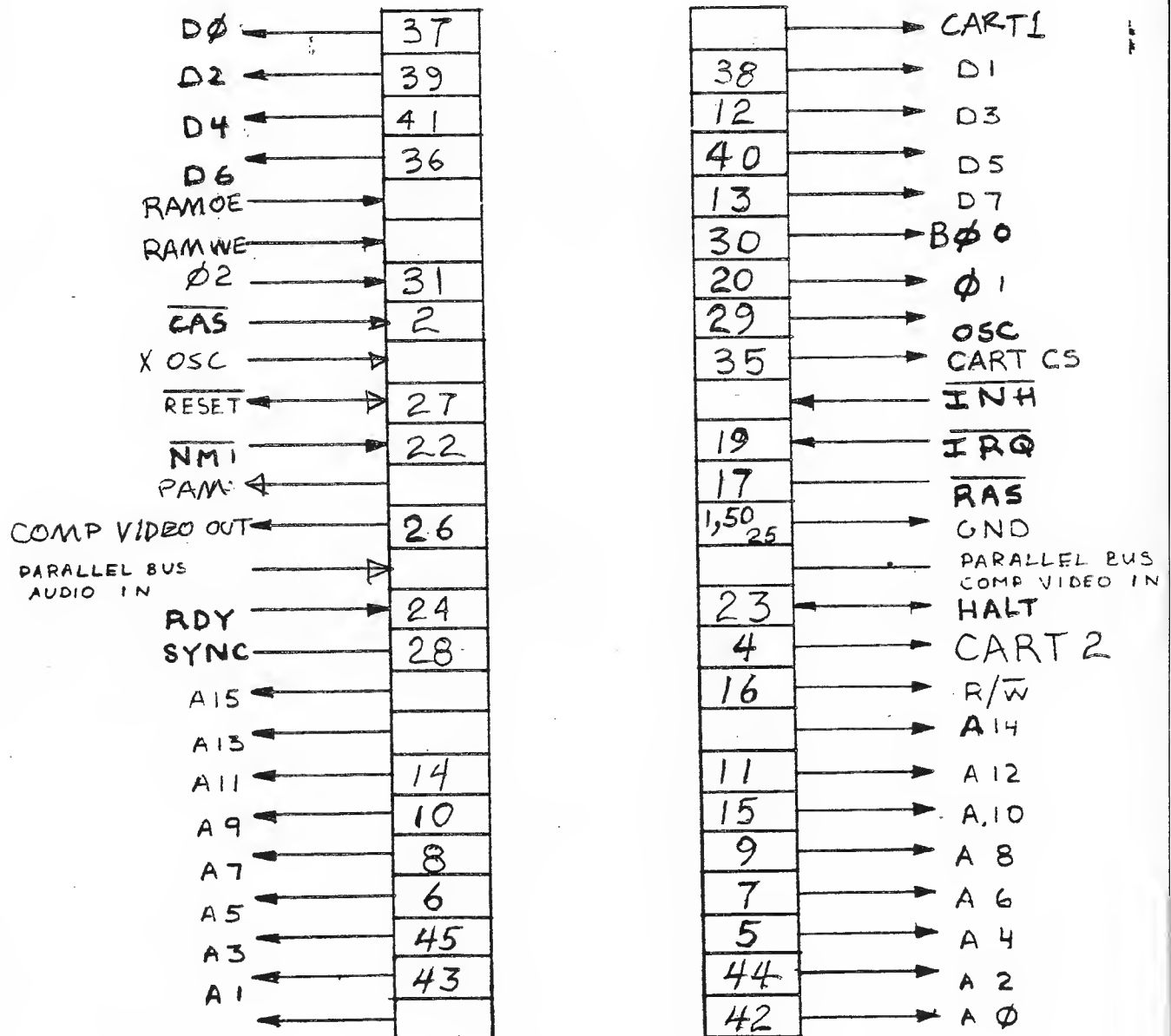
Frequency Range: 100Hz to 100KHz

ATARI 600 Computer System Block Diagram



Total on-board memory: 88K in 64K RAM version

Preliminary Parallel Bus



Pin Assignments
not firm

CRAZY 8: PARTS COST SUMMARY*

VERSION DATE: JANUARY 7, 1983

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PLUS: DUTIES, SHIPPING, OVERHEAD, AND LABOR (.55 HOURS FINAL
ASSEMBLY AND TEST)

* REVISED VERSION ON 1/14/83

RESISTORS

RESISTORS

ITEM #	PART #	QUANTITY	UNIT COST	TOTAL COST	DESCRIPTION	DESIGNATION	NOTES/SOURCE
1	14-5101	2	.0034	.0068	100ohm, .25W, 5%	R32, 34	RESIST. PRICES BY M. STRUTZEL, VAL PROJ.
2	T80	1	.0034	.0034	27ohm, .25W, 5%	R36	
3	14-5474	1	.0034	.0034	470ohm, .25W, 5%	R47	
4	14-5182	5	.0034	.017	1.8K, .25W, 5%	R4, 16, 39, 63, 64	
5	14-5472	13	.0034	.0442	4.7K, .25W, 5%	R3, 8, 21, 51-53, 55-59, 62, 69	
6	14-5102	11	.0034	.0374	1K, .25W, 5%	R1, 5, 9, 15, 42-4660, 61	
7	14-5103	3	.0034	.0102	10K, .25W, 5%	R2, 7, 11	
8	T80	7	.0034	.0238	T80	R40, 41, 65-68, 70	
9	14-5183	3	.0034	.0102	18K, .25W, 5%	R12, 19, 71	
10	14-5332	1	.0034	.0034	3.3K, .25W, 5%	R6	
11	14-5912	2	.0034	.0068	9.1K, .25W, 5%	R20, 28	
12	14-5222	1	.0034	.0034	2.2K, .25W, 5%	R18	
13	14-5363	1	.0034	.0034	36K, .25W, 5%	R22	
14	14-5331	3	.0034	.0102	330ohm, .25W, 5%	R26, 30, 31	
15	14-5392	1	.0034	.0034	3.9K, .25W, 5%	R27	
16	14-5105	1	.0034	.0034	1M, .25W, 5%	R25	
17	14-5104	3	.0034	.0102	100K, .25W, 5%	R24, 35, 38	
18	14-5272	2	.0034	.0068	2.7K, .25W, 5%	R29, 54	
19	T80	1	.0034	.0034	1.5K, .25W, 5%	R33	
23	T80	1	.0034	.0034	6.8K, .25W, 5%	R10	
24	T80	1	.0034	.0034	15K, .25W, 5%	R13	
25	T80	1	.0034	.0034	12K, .25W, 5%	R14	
26	T80	1	.0034	.0034	91K, .25W, 5%	R17	
27	T80	1	.0034	.0034	470K, .25W, 5%	R23	
28	T80	2	.0034	.0068	220K, .25W, 5%	R37, 49	
29	19-411504	1	.13	.13	500K, .25W, 5%	R50	TRIMPOT
30	T80	1	.0034	.0034	3K, .25W, 5%	R48	
TOTALS: 71				.368			

CAPACITORS

CAPACITORS

ITEM #	PART #	QUANTITY	UNIT COST	TOTAL COST	DESCRIPTION	DESIGNATION
31	CO-14181-03	16	.052	.832	.1mf, +80-20%, 75U, CER AX	C1, 8, 13, 23, 32, 45
32	CO-14181-02	6	.03	.18	.01mf, +80-20%, 75U, CER AX	C14, 15, 19, 20, 25, 27, 41-44, 46, 55, 56, 81, 84-91
33	CO-14181-01	3	.028	.084	.001mf, +80-20%, 75U, CER AX	C21, 35, 37
34	CO-14181-07	1	.04	.04	.47uf, +80-20%, 75U, CER AX	C29
35	CO-14170-02	4	.079	.316	47pf, +80-20%, 75U, CER AX	C24, 39, 82, 83
36	CO-10821	1	.081	.081	POLY, 820pf, 5%	C18A
37	CO-14180-03	2	.027	.054	100pf, 20%, X7R, CER AX	C17, C36
38	CO-14179-03	2	.079	.158	10pf, +20%, NPQ	C16, C28
39	CO-14179-04	1	.03	.03	33uf, C06	C26
40	CO-14374-02	1	.68	.68	4700uf, ELECTRO, +5-10%	C30
41	CO-14181-05	1	.04	.04	.22uf, 20%	C31
42	CO-14371	1	.053	.053	10uf, 16V, +50-10%	C33
43	T80	1	.049	.049	68pf,	C38
44	T80	1	.038	.038	15pf,	C40
45	CO-14180-05	1	.081	.081	220pf	C18
46	T80	1	.113	.113	.047uf	C22

TOTALS: 43

2.829

CONNECTORS AND SWITCHES

CONNECTORS AND SWITCHES

ITEM #	PART #	QUANTITY	UNIT COST	TOTAL COST	DESCRIPTION	DESIGNATION
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47	TBD	1	.78	.78	SERIAL BUSS CONNECTOR	J5
48	CO-14715	1	.31	.31	CONNECTOR, POWER JACK	J6
49	CO-10448	2	.28	.56	CONN, 9PIN-D*, RT ANG, JST	J1,2
50	CO-14715	1	.77	.77	CART CONN, 30PIN	J4
51	79-5903	1	.125	.125	RCA PHONO JACK, RT ANG	J3
52	CO12241	1	.095	.095	CHAN SELECT	S1,2
53	CO-14386-09	5	.144	.72	SOCKETS, 40PIN	U2,7-9,12
54	CO-14386-08	2	.1	.2	SOCKETS, 28PIN	U1,11
55	CO-14386-03	2	.06	.12	SOCKETS, 16PIN	U3,10,21
56	TBD	1	.1	.1	KEYBOARD CONNECTOR	U6,U20
57	CO-14386-05	1	.072	.072	SOCKETS, 20PIN	(64K ONLY) U23
58	CO14397-XX	1	.35	.35	PWR SWITCH	
59	TBD	18		0	SOCKETS, 18PIN	U14-19
60	TBD	1		0	SOCKETS, 48PIN	U13
61	TBD	1	6.6	6.6	PCB, CRAZY 8	

TOTALS: 39

10.802

A.e1 SHINI: .15 THIS ITEM

LSI SOCKETED ONLY
ALL SOCKETS MAY BE DELETED

TAIWAN; NO GOLD USED; BASED ON 2600 COST

INCLUDES PCB

IC's

IC's

ITEM #	PART #	QUANTITY	UNIT COST	TOTAL COST	DESCRIPTION	DESIGNATION
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62	TBD	1	3.85	3.85	FRED CHIP, 48 PIN	U13
63	CO-12294-A	1	2.5	2.5	PORKY CHIP, 40 PIN	U12
64	CO-14806	1	3.25	3.25	SALLY CHIP (MOD. 6502)	U9
65	CO-12296	1	3.57	3.57	ANTIC CHIP	U8
66	CO-14805	1	2.54	2.54	BTIA	U7
67	MK-2764	1	2.5	2.5	ROM:8K*8	BASIC ROM
68	CO-14795	1	1.82	1.82	PIA	U1
69	SS-60473	2	4.75	9.5	RAM 16K*4	U2
70	S-23128	1	5.8	5.8	RUFUS CHIP (16K*8)	U14,15
71	CD-4050B	1	.17	.17	HEX CHOS BUFFER; CD4050B	U11
72	7805	1	.35	.35	VOLT.REGULATOR	U4
73	CD-4051	2	.18	.36	HEX CHOS BUFFER	
74	CO14344	0	.26	0	74LS138	U20
75	TBD	1	.271	.271	LM3806(RF)	U6
TOTALS: 15				36.481	16K VERSION	

6.SUMMER

6.SUMMER: 4.50 UNIT COST

6.SUMMER: 5.00 UNIT COST

UNIT COST ESTIMATED

EST '84 COST (80% OF '83 COST)

29.415

MCCLINTOCK: EST '84 SI 70% '83

25.882

MISC. ELECTRICAL				MISC. ELECTRICAL			
ITEM #	PART #	QUANTITY	UNIT COST	TOTAL COST	DESCRIPTION	DESIGNATION	
76	34-2N3904	2	.049	.098	TRANSISTORS: 2N3904	Q1, Q4	
77	33-2N3906	3	.043	.129	TRANSISTORS: 2N3906	Q5, 6, 7	
78	34-2N3963	1	.06	.06	TRANSISTORS: 2N3963	Q2	
79	MR501	4	.105	.42	DIODES(BRIDGE RECT)	CR 3-6	
80	CO-14776	1	.08	.08	L.E.D.	CR8	
81	31-1N914	3	.015	.045	DIODE: RF	CR1, 2, 8	
82	CO-14384	5	.025	.125	INDUCTOR:FERRITE BEAD	L6-8, 11, 12	
83	SS-61090	1	.5	.5	CRYSTAL: 14.31818 MHz	X1	
84		0	0	0			HONG KONG ESTIMATE .35
85		0	0	0			
86	CO10823	2	.068	.136	INDUCTOR, VARIABLE	L3, 9	
87	TBD	63	.0034	.2142	SIP RESISTORS	SIP 1-7	
88	TBD	36	.028	1.008	SIP CAPACITORS	SIP 8-11	
89	TBD	1	.045	.045	TRANSFORMER, RF		
TOTALS: 122				2.8602			

MECHANICAL				MECHANICAL			
ITEM #	PART #	QUANTITY	UNIT COST	TOTAL COST	DESCRIPTION	DESIGNATION	
90	SS-60581	1	.584	.584	HEATSINK, REGULATOR		ALPS PRICE
91	TBD	1	8	8	KEYBOARD		
92	TBD	2	1	2	PLASTIC HOUS, TOP & BOT		
93	TBD	1	.7	.7	RF SHIELD, BOTTOM		
94	TBD	4	.003	.012	RUBBER FEET		
95	TBD	1	.03	.03	FCC LABEL		
96	X	X	X	.25	MISC HARDWARE		
TOTALS: 10				11.576			

PACKOUT

PACKOUT

ITEM #	PART#	QUANTITY	UNIT COST	TOTAL COST	DESCRIPTION	DESIGNATION
97	C014744	1	.05	.05	POLY BAG	
98	TBD	1	.8	.8	OPER MANUAL, INCL BAS&OWN	
99	C017710	1	.17	.17	WARRANTY CARD	
100	C017535	1	.22	.22	ATARI PCS PRODUCT GUIDE	
101	C015936	1	.03	.03	PUBL. QUEST.	
102	TBD	1	.01	.01	PCB SERIAL # LABEL	
103	TBD	1	.5	.5	SHIPPING CARTON, INNER	
104	TBD	1	.5	.5	SHIPPING CARTON, W/PRINTING	
105	CA0-17964	1	3.41	3.41	POWER ADAPT. 15-25 V/A	
106	SSA-61013	1	.8	.8	CABLE ASSY, COAX WITH TORROID	
107	TBD	1	.55	.55	TV SWITCH BOX	
TOTALS: 11				7.04		
GRAND TOTALS: 311				71.9562		
				'84 EST: 64.8902	(SI COST DOWN 20%)	

ORIENT ESTIMATE \$2.00

117/83

Production Start Goal

[illegible]

1/7/83

EL A

[illegible]

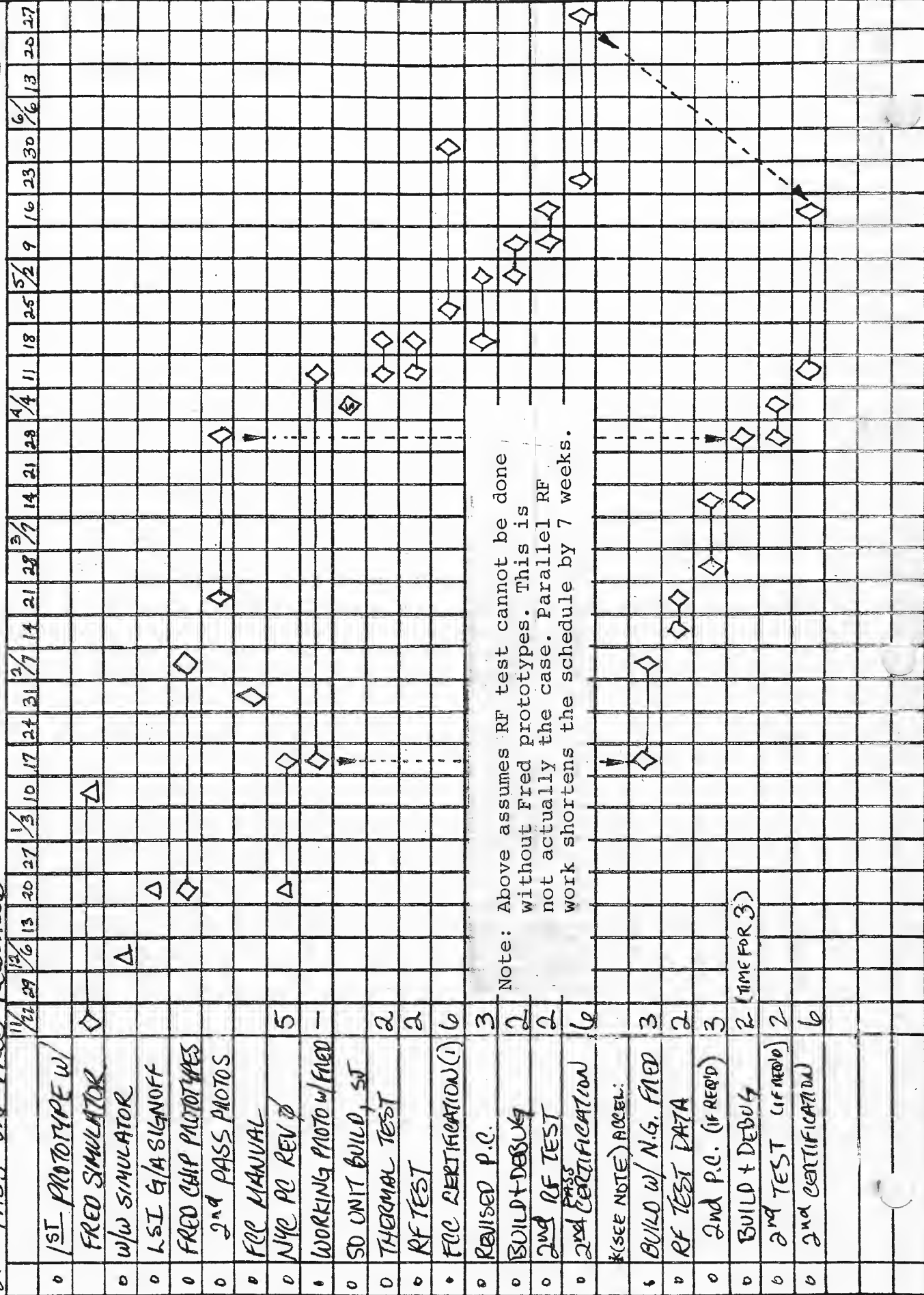
LIZ ELECTRICAL

G. SQUIRES (212) 309-0001

1/1/83

2ND PASS ON FRED REQUIRED

E10



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Corporate Research

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